spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile calculating circuit generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory circuit when said timer value is less than a first communication stop time interval threshold value on staring of a re-communication, said known signal replica generating circuit making said delay profile calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

6. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

a spreading timing controlling circuit, connected to said spreading code and spreading timing memory circuit, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said communication stop time interval threshold value on starting of the re-communication.

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